AMENDMENTS TO THE CLAIMS

Claims 1-57 are cancelled.

58. (Currently Amended) A method for placing cells of a netlist, comprising the steps of:

receiving said netlist which describes a circuit to be fabricated on a semiconductor chip, said netlist specifying a particular group of cells and wire connections between said cells;

receiving a specification of a placement area describing a plurality of sites on said semiconductor chip where said cells may reside;

performing a coarse placement process which assigns initial locations to said cells using floating point coordinates for cell locations;

performing a detailed placement process which assigns a legal location to each of said cells by snapping a cell from its floating point coordinates to a nearest legal location;

performing a synthesis process.

59. (Previously Presented) The method of Claim 58, wherein the detailed placement process is limited to only performing legalization such that said cells are assigned to legal sites without violating constraints set forth in said specification of said placement area.

60. (Currently Amended) The method of Claim 59, wherein

said detailed placement process ~~snaps cells into said legal sites~~ includes resolving any overlapping cells.

61. (Currently Amended) The method of Claim 59, wherein said detailed placement process ~~moves cells a minimum distance to achieve said legalization~~ includes defining a master objective function to evaluate a goodness of a cell placement.

62. (Previously Presented) The method of Claim 58 further comprising the step of iterating said detailed placement process and said synthesis process a plurality of times.

63. (Previously Presented) The method of Claim 58, wherein said synthesis process is timing driven.

64. (Previously Presented) The method of Claim 58, wherein said coarse placement process is congestion driven.

65. (Currently Amended) A method for placing cells of a netlist, comprising the steps of:

performing a detailed placement process which ~~is limited to only assigning legal locations to said cells~~ includes snapping a cell from floating point coordinates to a nearest legal location;

performing a synthesis process;

repeating said detailed placement process and said synthesis process a plurality of times for convergence.

66. (Cancelled)

67. (Cancelled)

68. (Previously Presented) The method of Claim 65, wherein said synthesis process is timing driven.

69. (Previously Presented) The method of Claim 65 further comprising the step of performing a coarse placement process before said detailed placement process and said synthesis process.

70. (Previously Presented) The method of Claim 69, wherein said coarse placement process minimizes wire length.

71. (Currently Amended) A method for placing cells of a netlist, comprising the steps of:

performing a detailed placement process having a primary function of legalization, wherein ~~said cells are placed in legal sites~~ a cell is snapped to its nearest legal site;

performing a synthesis process, wherein said ~~synthesize~~ synthesis process is timing driven;

integrating the detailed placement process with the

synthesis process.

72. (Previously Presented) The method of Claim 71, wherein the detailed placement process only performs legalization.

73. (Cancelled)

74. (Cancelled)

75. (Previously Presented) The method of Claim 71, wherein said detailed placement process and said synthesis process are integrated by iteratively repeating said detailed placement process and said synthesis process a plurality of times to achieve convergence.

76. (Previously Presented) The method of Claim 71 further comprising the step of performing congestion driven placement.

77. (Previously Presented) The method of Claim 71, wherein said synthesis process minimizes wire length.

78. (Previously Presented) A method for placing cells of a netlist, comprising the steps of:

receiving the netlist, wherein the netlist describes a circuit to be fabricated on a semiconductor chip, and wherein the netlist specifies a particular group of cells and wire connections between the cells;

receiving a specification of a placement area describing a plurality of sites on the semiconductor chip where the cells may

reside, wherein a circuit density of a ratio of total cells area to total available site area is one hundred percent;

performing a coarse placement process that assigns initial locations to the cells; and

performing a detailed placement process that assigns a final location to each of the cells by optimizing a cost function dependent on the sites in pairs of rows, thereby allowing swapping of cells between the pairs of rows based on the cost function, wherein each cell location is aligned with a valid site boundary, wherein no two cells are overlapping, and wherein each cell is assigned to a group of legal sites so that each cell is placed on the legal sites without violating constraints set forth in the specification of the placement area.

79. (Previously Presented) The method of Claim 78, wherein the detailed placement process runs in linear time.

80. (Previously Presented) The method of Claim 78, wherein the detailed placement process further comprises the step of using a dynamic programming technique to perform the swapping of cells between the pairs of rows.

81. (Currently Amended) The method of Claim 78, wherein a look-ahead parameter is used to control ~~usages of cell~~ swapping of cells between pairs of rows.

82. (Previously Presented) The method of Claim 78, wherein the detailed placement process further comprises pruning a search space during using a dynamic programming technique to perform the swapping of cells between the pairs of rows.

83. (Previously Presented) The method of Claim 82, wherein the pruning step is controlled as a function of a gap count.

84. (Previously Presented) The method of Claim 78, wherein the detailed placement process uses a subroutine that finds an optimal legal cell location assignment for a single row in an absence of blockages.

85. (Previously Presented) The method of Claim 78, wherein the detailed placement process further comprises the step of assigning an initial cell location based on a result of the coarse placement process.

86. (Previously Presented) The method of Claim 85, wherein the coarse placement process uses conjugate gradient method.

87. (Previously Presented) The method of Claim 85, wherein the detailed placement process further comprises optimizing a y-location of the cells during initial cell location assignment.

88. (Currently Amended) The method of Claim 87, wherein ~~the~~ optimizing ~~step~~ the y-location of the cells during initial cell location assignment is performed through a dynamic programming technique.

89. (Previously Presented) The method of Claim 88, wherein the detailed placement process further comprises the step of performing a greedy cleanup phase.

90. (Previously Presented) A method for placing cells of a netlist, comprising the steps of:

receiving the netlist, wherein the netlist describes a circuit to be fabricated on a semiconductor chip, and wherein the netlist specifies a particular group of cells and wire connections between the cells;

receiving a specification of a placement area describing a plurality of sites on the semiconductor chip where the cells may reside;

performing a coarse placement process that assigns initial locations to the cells;

performing a detailed placement process that assigns a final location to each of the cells by optimizing a cost function dependent on the sites in pairs of rows, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that the each cell is placed on the legal sites without violating constraints set forth in the specification to the placement area; and

using a dynamic programming technique to perform a swapping of cells between the pairs of rows based on the cost function.

91. (Previously Presented) The method of Claim 90, wherein the detailed placement process runs in linear time.

92. (Previously Presented) The method of Claim 90, wherein a circuit density of a ratio of total cell area to total available site area is one hundred percent.

93. (Previously Presented) The method of Claim 90, wherein a look-ahead parameter is used to control usages of the swapping of cells between pairs of rows.

94. (Previously Presented) The method of Claim 90, wherein the detailed placement process further comprises the step of pruning a search space during the dynamic programming process.

95. (Previously Presented) The method of Claim 94, wherein the pruning step is controlled as a function of a gap count.

96. (Previously Presented) The method of Claim 90, wherein the detailed placement process uses a subroutine that finds an optimal legal cell location assignment for a single row in an absence of blockages.

97. (Previously Presented) The method of Claim 90, wherein the detailed placement process further comprises the step of assigning an initial cell location based on a result of the coarse placement process.

98. (Previously Presented) The method of Claim 97, wherein the coarse placement process uses conjugate gradient method.

99. (Previously Presented) The method of Claim 97, wherein the detailed placement process further comprises the step of optimizing a y-location of the cells during the initial cell location assignment.

100. (Currently Amended) The method of Claim 99, wherein ~~the~~ optimizing ~~step~~ the y-location of the cells during the initial cell location assignment is performed through the dynamic programming technique.

101. (Previously Presented) The method of Claim 100, wherein the detailed placement process further comprises the step of performing a greedy cleanup phase.

102. (Previously Presented) A method of placing cells of a netlist, comprising the steps of:

receiving the netlist, wherein the netlist describes a circuit to be fabricated on a semiconductor chip, and wherein the netlist specifies a particular group of cells and wire connections between the cells;

receiving a specification of a placement area describing a plurality of sites on the semiconductor chip where the cells may reside;

performing a coarse placement process that assigns initial locations to the cells according to conjugate gradient process; and

performing a detailed placement process that assigns a final location to each of the cells by optimizing a cost function dependent on the sites in pairs of rows, thereby allowing swapping of cells between the pairs of rows based on the cost function, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that the each cell is placed on the legal sites without violating constraints set forth in the specification of the placement area.

103. (Previously Presented) The method of Claim 102, wherein the detailed placement process runs in linear time.

104. (Previously Presented) The method of Claim 102, wherein a circuit density of a ratio of total cell area to total available site area is one hundred percent.

105. (Previously Presented) The method of Claim 102, wherein a look-ahead parameter is used to control usages of the swapping of cells between pairs of rows.

106. (Previously Presented) The method of Claim 102, wherein the detailed placement process further comprises the step of pruning a search space during a dynamic programming process for the swapping of cells between the pairs of rows based on the cost function.

107. (Previously Presented) The method of Claim 106, wherein the pruning step is controlled as a function of a gap count.

108. (Previously Presented) The method of Claim 102, wherein the detailed placement process uses a subroutine that finds an optimal legal cell location assignment for a single row in an absence of blockages.

109. (Previously Presented) The method of Claim 108, wherein the detailed placement process further comprises the step of assigning an initial cell location based on a result of the coarse placement process.

110. (Previously Presented) The method of Claim 109, wherein the detailed placement process further comprises the step of optimizing a y-location of the cells during the initial cell location assignment.

111. (Currently Amended) The method of Claim 110, wherein ~~the~~ optimizing ~~step~~ the y-location of the cells during the

initial cell location assignment is performed through the dynamic programming technique.

112. (Previously Presented) The method of Claim 111, wherein the detailed placement process further comprises the step of performing a greedy cleanup process.

113. (Previously Presented) A method of placing cells of a netlist, comprising the steps of:

receiving the netlist, wherein the netlist describes a circuit to be fabricated on a semiconductor chip, and wherein the netlist specifies a particular group of cells and wire connections between the cells;

receiving a specification of a placement area describing a plurality of sites on the semiconductor chip where the cells may reside;

performing a coarse placement process that assigns initial locations to the cells;

performing a detailed placement process that assigns a final location to each of the cells by optimizing a cost function dependent on the sites in pairs of rows, thereby allowing swapping of cells between the pairs of rows based on the cost function, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that the each cell is placed on the legal sites without violating constraints set forth in the specification of the placement area; and

using a subroutine that legalizes a single row optimally according to a sum of squares objective in linear, quadratic, or polynomial run time.

114. (Previously Presented) A method for placing cells of a netlist, comprising the steps of:

receiving the netlist, wherein the netlist describes a circuit to be fabricated on a semiconductor chip, and wherein the netlist specifies a particular group of cells and wire connections between the cells;

receiving a specification of a placement area describing a plurality of sites on the semiconductor chip where the cells may reside;

performing a coarse placement process that assigns initial locations to the cells;

performing a detailed placement process that assigns a final location to each of the cells by optimizing a cost function dependent on the sites in pairs of rows, thereby allowing swapping of cells between the pairs of rows based on the cost function, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that the each cell is placed on the legal sites without violating constraints set forth in the specification of the placement area; and

using a subroutine that legalizes a single row optimally for a given fixed cell ordering in linear, quadratic, or polynomial run time.

115. (Previously Presented) A method of placing cells of a netlist, comprising the steps of:

receiving the netlist, wherein the netlist describes a circuit to be fabricated on a semiconductor chip, and wherein the netlist specifies a particular group of cells and wire connections between the cells;

receiving a specification of a placement area describing a plurality of sites on the semiconductor chip where the cells may reside;

performing a coarse placement process that assigns initial locations to the cells;

performing a detailed placement process that assigns a final location to each of the cells by optimizing a cost function dependent on the sites in pairs of rows, thereby allowing swapping of cells between the pairs of rows based on the cost function, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that the each cell is placed on the legal sites without violating constraints set forth in the specification of the placement area; and

legalizing a single row optimally using a dynamic programming technique for the swapping of cells between the pairs of rows based on the cost function.

116. (Previously Presented) A method for placing cells of a netlist, comprising the steps of:

receiving the netlist, wherein the netlist describes a circuit to be fabricated on a semiconductor chip, and wherein the netlist specifies a particular group of cells and wire connections between the cells;

receiving a specification of a placement area describing a plurality of sites on the semiconductor chip where the cells may reside;

performing a coarse placement process that assigns initial locations to the cells;

performing a detailed placement process that assigns a final location to each of the cells by optimizing a cost function dependent on the sites in pairs of rows, thereby

allowing swapping of cells between the pairs of rows based on the cost function, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that the each cell is placed on the legal sites without violating constraints set forth in the specification of the placement area; and

using a subroutine that legalizes two rows optimally according to a sum of squares objective in quadratic or polynomial run time.

117. (Previously Presented) A method of placing cells of a netlist, comprising the steps of:

receiving the netlist, wherein the netlist describes a circuit to be fabricated on a semiconductor chip, and wherein the netlist specifies a particular group of cells and wire connections between the cells;

receiving a specification of a placement area describing a plurality of sites on the semiconductor chip where the cells may reside;

performing a coarse placement process that assigns initial locations to the cells;

performing a detailed placement process that assigns a final location to each of the cells by optimizing a cost function dependent on the sites in pairs of rows, thereby allowing swapping of cells between the pairs of rows based on the cost function, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that the each cell is placed on the legal sites without violating constraints set forth in the specification of the placement area; and

using a subroutine that legalizes two rows optimally for a given fixed cell ordering in quadratic or polynomial run time.

118. (Currently Amended) A method of placing cells of a netlist, comprising the steps of:

receiving the netlist, wherein the netlist describes a circuit to be fabricated on a semiconductor chip, and wherein the netlist specifies a particular group of cells and wire connections between the cells;

receiving a specification of a placement area describing a plurality of sites on the semiconductor chip where the cells may reside;

performing a coarse placement process that assigns initial locations to the cells;

performing a detailed placement process that assigns a final location to each of the cells by optimizing a cost function dependent on the sites in pairs of rows, thereby allowing swapping of cells between the pairs of rows based on the cost function, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that the each cell is placed on the legal sites without violating constraints set forth in the specification of the placement area; and

legalizing two rows optimally using a dynamic programming technique for the swapping of cells between the pairs of rows based on the cost function.

119. (Previously Presented) A method for placing cells of a netlist, comprising the steps of:

receiving the netlist, wherein the netlist describes a circuit to be fabricated on a semiconductor chip, and wherein the netlist specifies a particular group of cells and wire connections between the cells;

receiving a specification of a placement area describing a plurality of sites on the semiconductor chip where the cells may reside;

performing a coarse placement process that assigns initial locations to the cells;

performing a detailed placement process that assigns a final location to each of the cells by optimizing a cost function dependent on the sites in pairs of rows, thereby allowing swapping of cells between the pairs of rows based on the cost function, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that the each cell is placed on the legal sites without violating constraints set forth in the specification of the placement area; and

using a subroutine that legalizes a pair of rows optimally according to y-displacement metric in quadratic or polynomial time.

120. (Previously Presented) A method for placing cells of a netlist, comprising the steps of:

receiving the netlist, wherein the netlist describes a circuit to be fabricated on a semiconductor chip, and wherein the netlist specifies a particular group of cells and wire connections between the cells;

receiving a specification of a placement area describing a plurality of sites on the semiconductor chip where the cells may reside;

performing a coarse placement process that assigns initial locations to the cells;

performing a detailed placement process that assigns a final location to each of the cells by optimizing a cost function dependent on the sites in pairs of rows, thereby

allowing swapping of cells between the pairs of rows based on the cost function, wherein each cell location is aligned with a valid site boundary, no two cells are overlapping, and each cell is assigned to a group of legal sites so that the each cell is placed on the legal sites without violating constraints set forth in the specification of the placement area; and

using a subroutine that legalizes N rows optimally according to a y-displacement metric in quadratic or polynomial run time.

CONCLUSION

Claims 58-65, 68-72, and 75-120 are pending in the present Application. Applicants respectfully request allowance of these claims.

If there are any questions, please telephone the undersigned at 408-451-5907 to expedite prosecution of this case.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as FIRST CLASS MAIL in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on March 9, 2005.

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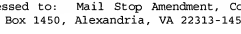

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